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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,858	12/02/2003	Paul Walker	1801270.00133US1	5600

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EXAMINER	
DAY, HERNG DER	
ART UNIT	**PAPER NUMBER**
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	01/16/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 01/16/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/726,858	WALKER, PAUL	
	Examiner	Art Unit	
	Herng-der Day	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-19 and 21-30* is/are rejected.

7)☒ Claim(s) *10 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/30/04,1/17/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 have been examined.

Priority

2. Acknowledgment is made of Applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copies have been filed in parent Application No. 0315350.9, filed on June 28, 2003 and in parent Application No. 0322325.2, filed on September 24, 2003.

Specification

3. The disclosure is objected to because of the following informalities. Appropriate correction is required.

3-1. It appears that "processors 12 and 24", as described in line 5 of paragraph [0015], should be "processors 12 and 22".

3-2. As described at lines 3-4 of paragraph [0019], "if the architecture pf the target machine 2". (Emphasis added.)

3-3. A period is missing at the end of paragraph [0024].

3-4. As described at line 2 of paragraph [0041], "thus man(x) it 53 bits wide". (Emphasis added.)

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 21-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5-1. Claim 21 recites the limitation "In combination" in line 1 of the claim. It is vague and indefinite because it is unclear what the meaning of "In combination" is.

5-2. Claims 22-30 are rejected as being dependent on a rejected claim.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claims 21-30 are rejected under 35 U.S.C. 101 because the inventions as disclosed in claims are directed to non-statutory subject matter.

7-1. Claims 21-30 recite "combination" and are non-statutory for failing to be in one of the categories of patentable invention.

Claim Objections

8. Claims 1, 2, 11, 12, 21, and 22 are objected to because there is no period at the end of each claim. Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-9, 11-19, and 21-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Arakawa et al., "SH4 RISC Multimedia Microprocessor", IEEE Micro, Volume 18, Issue 2, March-April 1998, pages 26-34 (IDS AD filed January 17, 2006).

10-1. Regarding claim 1, Arakawa et al. disclose a method of performing high precision emulation of program code instructions for a subject machine on a target machine, comprising:

determining if operands in instructions of the program code for the subject machine (double-precision instructions, page 33, left column, paragraph 4) require a different precision than provided for by the target machine (single-precision hardware, page 33, left column, paragraph 4); and

applying a floating point emulation algorithm to perform intermediate calculations on the operands of the instructions at a higher precision than the precision supported by the target machine (The double-precision instructions are emulated with single-precision hardware, page 33, left column, paragraph 4).

10-2. Regarding claim 2, Arakawa et al. further disclose wherein the target machine includes floating point hardware and integer hardware, wherein said floating point emulation algorithm comprises:

utilizing floating point hardware on the target machine to perform calculations on the operands of the instructions when it is determined based upon the intermediate calculations that the target machine provides sufficient precision for the calculations required by the instructions; and utilizing integer hardware on the target machine to perform calculations not selected to be performed by the floating point hardware (The SH architecture has floating-point and integer multiply-accumulate instructions, and the hardware for these instructions can also be used for double-precision instruction emulation, page 33, left column, paragraph 4).

10-3. Regarding claim 3, Arakawa et al. further disclose wherein the program code instructions are accumulated instructions that are calculated at a higher precision than the operands capable of being handled by the target machine (The SH architecture has floating-point and integer multiply-accumulate instructions, and the hardware for these instructions can also be used for double-precision instruction emulation, page 33, left column, paragraph 4).

10-4. Regarding claim 4, Arakawa et al. further disclose wherein the program code instructions are floating point accumulated instructions of the form: $d = \pm(a*b \pm c)$, wherein a, b, c and d are operands expressible as floating point numbers (multiply-accumulate instructions, page 33, left column, paragraph 4).

10-5. Regarding claim 5, Arakawa et al. further disclose comprising identifying whether any of the operands (a, b, or c) are special values having a known result that all compatible hardware will produce regardless of the level of precision of said hardware (The SH4 ... must support the double-precision format and conform to the ANSI/IEEE 754 standard, page 33, left column, paragraph 3; identifying special values is within the standard).

10-6. Regarding claim 6, Arakawa et al. further disclose wherein said special values include either zero, infinity, or NaN (not a number), wherein the floating point hardware is utilized to calculate the result of the accumulated instructions when any of the operands (a, b, or c) are identified as special values (The SH4 ... must support the double-precision format and conform to the ANSI/IEEE 754 standard, page 33, left column, paragraph 3; calculating result when operands have special values is within the standard).

10-7. Regarding claim 7, Arakawa et al. further disclose wherein said floating point emulation algorithm further comprises:

determining whether the exponent for the result of the multiplication of (a*b) overlaps with the exponent of c; and utilizing the floating point hardware to calculate the result of the accumulated instructions when the exponent for the result of the multiplication of (a*b) fails to overlap with the exponent of c (The SH4 ... must support the double-precision format and conform to the ANSI/IEEE 754 standard. ... The SH architecture has floating-point and integer multiply-accumulate instructions, and the hardware for these instructions can also be used for double-precision instruction emulation, page 33, left column, paragraphs 3-4).

10-8. Regarding claim 8, Arakawa et al. further disclose wherein, when the exponent for the result of the multiplication of (a*b) overlaps with the exponent of c, said floating point emulation algorithm further comprising:

determining whether the mantissa for the result of the multiplication (a*b) requires more mantissa bits than provided for by said floating point hardware; and utilizing the floating point hardware to calculate the result of the accumulated instructions when the result of the multiplication (a*b) does not require more mantissa bits than provided for by the floating point

hardware (The SH4 ... must support the double-precision format and conform to the ANSI/IEEE 754 standard. ... The SH architecture has floating-point and integer multiply-accumulate instructions, and the hardware for these instructions can also be used for double-precision instruction emulation, page 33, left column, paragraphs 3-4).

10-9. Regarding claim 9, Arakawa et al. further disclose said floating point emulation algorithm further comprising computing the full calculation of a*b using the integer hardware when mantissa for the result of the multiplication (a*b) requires more mantissa bits than provided for by the floating point hardware (Double-precision multiply, page 33, Figure 10).

10-10. Regarding claims 11-19, these medium claims include equivalent method limitations as in claims 1-9 and are anticipated using the same analysis of claims 1-9.

10-11. Regarding claims 21-29, these combination claims include equivalent method limitations as in claims 1-9 and are anticipated using the same analysis of claims 1-9.

Allowable Subject Matter

11. Claims 10 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

Reference to Trissel et al., U.S. Patent 5,341,320 issued August 23, 1994, is cited as disclosing a method for processing exception conditions in a floating-point system.

Reference to Markstein et al., U.S. Patent 5,631,859 issued May 20, 1997, is cited as disclosing a floating point arithmetic unit having logic for quad precision arithmetic.

Reference to Dulong et al., U.S. Patent 6,163,764 issued December 19, 2000, is cited as disclosing techniques to emulate a double precision instruction set on a processor which has an expanded precision format representation.

Reference to Kelley et al., U.S. Patent 6,697,832 B1 issued February 24, 2004, and filed July 30, 1999, is cited as disclosing a floating-point processor with improved intermediate result handling.

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (571) 272-3777. The Examiner can normally be reached on 9:00 - 17:30.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: (571) 272-2100.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kamini S. Shah can be reached on (571) 272-2279. The fax phone numbers for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Herng-der Day
January 8, 2007 H.D.

KAMINI SHAH
SUPERVISORY PATENT EXAMINER